REVISIONS			
LTR	DESCRIPTION	DATE (YY-MM-DD)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Thanh V. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 02-12-18	**CHECKED BY** Thanh V. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/03610**
	REV	**PAGE** 1 **OF** 51

AMSC N/A

5962-V010-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance digital signal processor microcircuit, with an operating temperature range of -40°C to +100°C for device type 01 and -55°C to +125°C for device type 02 as shown in 1.2.1 below.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	320VC33-EP	Digital signal processor
02	320VC33-EP	Digital signal processor

1.2.2 Case outline(s). The case outlines shall be as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	144	MS-026	Plastic quad flatpack
Y	144		Ceramic ball grid array

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

1.3 Absolute maximum ratings. 1/

Supply voltage range (DV_{DD})	-0.3 V to +4.0 V 2/
Supply voltage range (CV_{DD})	-0.3 V to +2.4 V 2/
Input voltage range (V_I)	-1.0 V to +4.6 V 3/
Output voltage range (V_O)	-0.3 V to +4.6 V
Continuous power dissipation (worst case) (P_D)	500 mW 4/
Storage temperature range (T_{STG})	-55°C to +150°C 5/
Case operating temperature range (T_C):	
Device type 01	-40°C to +100°C
Device type 02	-55°C to +125°C

1.4 Recommended operating conditions. 2/ 6/ 7/ 8/

Supply voltage range for the core CPU (CV_{DD})	1.71 V to 1.89 V 9/
Supply voltage range for the I/O pins (DV_{DD})	3.0 V to 3.6 V 10/
Supply ground (V_{SS})	0.0 V
High level input voltage range (V_{IH})	0.7 x DV_{DD} to DV_{DD} + 0.3 V 3/
Low level input voltage range (V_{IL})	-0.3 V to 0.3 x DV_{DD} 3/
Maximum high level output current (I_{OH})	4.0 mA
Maximum low level output current (I_{OL})	4.0 mA
Case operating temperature range (T_C):	
Device type 01	-40°C to +100°C
Device type 02	-55°C to +125°C
Maximum capacitive load per output pin (C_L)	30 pF

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values are with respect to V_{SS}.

3/ Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of < 2 ns, < 10 mA, and < 1 V amplitude is permissable.

4/ Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the device, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{DD}) current specification in table I herein.

5/ Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

7/ All inputs and I/O pins are configured as inputs.

8/ All inputs and I/O pins use a Schmidt hysteresis inputs except $\overline{SHZ}$ and D0 – D31. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 x DV_{DD}.

9/ CV_{DD} should not exceed DV_{DD} by more than 0.7 V. (Use a Schottky clamp diode between these supplies.)

10/ DV_{DD} should not exceed CV_{DD} by more than 2.5 V.

2. APPLICABLE DOCUMENTS

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150 or at http://www.ieee.org).

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.4 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Functional block diagram. The functional block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 4.

3.5.5 Boundary scan instruction code. The boundary scan instruction code shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3.0 V ≤ DV_{DD} ≤ 3.6 V 1.71 V ≤ CV_{DD} ≤ 1.89 V unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	DV_{DD} = Min, I_{OH} = Max	25°C, -40°C to 100°C	01	2.4		V
			25°C, -55°C to 125°C	02	2.4		
Low level output voltage	V_{OL}	DV_{DD} = Min, I_{OL} = Max	25°C, -40°C to 100°C	01		0.4	V
			25°C, -55°C to 125°C	02		0.4	
High impedance current	I_Z	DV_{DD} = Max	25°C	All	-5.0	+5.0	µA
Input current	I_I	V_I = V_{SS} to DV_{DD}	25°C	All	-5.0	+5.0	µA
Input current (with internal pullup)	I_{IPU}	Inputs with internal pullups 3/	25°C, -40°C to 100°C	01	-600	10	µA
			25°C, -55°C to 125°C	02	-600	10	
Input current (with internal pulldown)	I_{IPD}	Inputs with internal pulldowns 3/	25°C, -40°C to 100°C	01	600	-10	µA
			25°C, -55°C to 125°C	02	600	-10	
Input current (with bus keeper) pullup 4/	I_{BKU}	Bus keeper opposes until conditions match	25°C, -40°C to 100°C	01	-600	10	µA
			25°C, -55°C to 125°C	02	-600	10	
Input current (with bus keeper) pulldown 4/	I_{BKD}		25°C, -40°C to 100°C	01	600	-10	µA
			25°C, -55°C to 125°C	02	600	-10	
Supply current, pins 5/ 6/	I_{DDD}	DV_{DD} = Max, f_X = 60 MHz	25°C	01		120	mA
		DV_{DD} = Max, f_X = 75 MHz	25°C	02		260	
Supply current, core CPU 5/ 6/	I_{DDC}	CV_{DD} = Max, f_X = 60 MHz	25°C	01		80	mA
		CV_{DD} = Max, f_X = 75 MHz	25°C	02		215	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
IDLE2, Supply current, I_{DDD} plus I_{DDC}	I_{DD}	PLL enabled, oscillator enabled	25°C, -40°C to 100°C	01	2 typical		mA
			25°C, -55°C to 125°C	02	2 typical		
		PLL disabled, oscillator enabled	25°C, -40°C to 100°C	01	500 typical		µA
			25°C, -55°C to 125°C	02	500 typical		
		PLL disabled, oscillator disabled, FLCK = 0	25°C, -40°C to 100°C	01	50 typical		
			25°C, -55°C to 125°C	02	50 typical		
Input capacitance 7/	C_I	All inputs except XIN	25°C	All		10	pF
		XIN input				10	
Output capacitance 7/	C_O		25°C	All		10	pF
Phase-locked loop characteristics using EXTCLK or on-chip crystal oscillator 8/							
Frequency range, PLL input 7/	F_{pllin}		25°C, -40°C to 100°C	01	5	15	MHz
			25°C, -55°C to 125°C	02	5	15	
Frequency range, PLL output 7/	F_{pllout}		25°C, -40°C to 100°C	01	25	75	MHz
			25°C, -55°C to 125°C	02	25	75	
PLL current, CV_{DD} supply 7/	I_{pll}		25°C, -40°C to 100°C	01		2	mA
			25°C, -55°C to 125°C	02		2	
PLL power, CV_{DD} supply 7/	P_{pll}		25°C, -40°C to 100°C	01		5	mW
			25°C, -55°C to 125°C	02		5	
PLL output duty cycle at H1 7/	PLL_{dc}		25°C, -40°C to 100°C	01	45	55	%
			25°C, -55°C to 125°C	02	45	55	
PLL output jitter, F_{pllout} = 25 MHz 7/	PLLJ		25°C, -40°C to 100°C	01		400	ps
			25°C, -55°C to 125°C	02		400	
PLL lock time in input cycles	PLL_{LOCK}		25°C, -40°C to 100°C	01		1000	cycles
			25°C, -55°C to 125°C	02		1000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Circuit parameters for on-chip crystal oscillator 9/							
Oscillator internal supply voltage	V_O	See figure 4	25°C, -40°C to 100°C	01	CV_{DD} typical		V
			25°C, -55°C to 125°C	02	CV_{DD} typical		
Fundamental mode frequency range 7/	F_O		25°C, -40°C to 100°C	01	1	20	MHz
			25°C, -55°C to 125°C	02	1	20	
DC bias point (input threshold) 7/	V_{bias}		25°C, -40°C to 100°C	01	40	60	$\%V_O$
			25°C, -55°C to 125°C	02	40	60	
Feedback resistance 7/	R_{fbk}		25°C, -40°C to 100°C	01	100	500	kΩ
			25°C, -55°C to 125°C	02	100	500	
Small signal ac output impedance 7/	R_{out}		25°C, -40°C to 100°C	01	250	1000	Ω
			25°C, -55°C to 125°C	02	250	1000	
The ac output voltage with test crystal 10/	V_{xoutac}		25°C, -40°C to 100°C	01	85 typical		$\%V_O$
			25°C, -55°C to 125°C	02	85 typical		
The ac input voltage with test crystal 10/	V_{xinac}		25°C, -40°C to 100°C	01	85 typical		$\%V_O$
			25°C, -55°C to 125°C	02	85 typical		
$V_{xin} = V_{xinh}$, $I_{xout} = 0$, $F_O = 0$ (logic input) 7/	V_{xoutl}		25°C, -40°C to 100°C	01	V_{SS} -0.1	V_{SS} +0.3	V
			25°C, -55°C to 125°C	02	V_{SS} -0.1	V_{SS} +0.3	
$V_{xin} = V_{xinl}$, $I_{xout} = 0$, $F_O = 0$ (logic input) 7/	V_{xouth}		25°C, -40°C to 100°C	01	CV_{DD} -0.3	CV_{DD} +0.1	V
			25°C, -55°C to 125°C	02	CV_{DD} -0.3	CV_{DD} +0.1	
When used for logic level input, oscillator enabled 7/	V_{inl}		25°C, -40°C to 100°C	01	-0.3	$0.2V_O$	V
			25°C, -55°C to 125°C	02	-0.3	$0.2V_O$	
When used for logic level input, oscillator enabled 7/	V_{inh}		25°C, -40°C to 100°C	01	$0.8V_O$	DV_{DD} +0.3	V
			25°C, -55°C to 125°C	02	$0.8V_O$	DV_{DD} +0.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Circuit parameters for on-chip crystal oscillator - Continued 9/								
When used for logic level input, oscillator disabled 7/	V_{xinh}	See figure 4		25°C, -40°C to 100°C	01	0.7 DV_{DD}	DV_{DD} +0.3	V
				25°C, -55°C to 125°C	02	0.7 DV_{DD}	DV_{DD} +0.3	
XOUT internal load capacitance 7/	C_{xout}			25°C	All	2	5	pF
XIN internal load capacitance 7/	C_{xin}			25°C	All	2	5	pF
Delay time, XIN to H1, x1 and x0.5 modes	$t_{d(XIN-H1)}$			25°C, -40°C to 100°C	01	2	8	ns
				25°C, -55°C to 125°C	02		8	
Input current, feedback enabled, $V_{il} = 0$ 7/	I_{inl}			25°C, -40°C to 100°C	01		50	µA
				25°C, -55°C to 125°C	02		50	
Input current, feedback enabled, $V_{il} = V_{ih}$ 7/	I_{inh}			25°C, -40°C to 100°C	01		-50	µA
				25°C, -55°C to 125°C	02		-50	
Timing requirements for EXTCLK, all modes								
Rise time, EXTCLK 7/	$t_{r(EXTCLK)}$	See figure 4	$F = F_{max}$, x0.5 and x1 modes	25°C, -40°C to 100°C	01		1	ns
				25°C, -55°C to 125°C	02		1	
			$F < F_{max}$	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Fall time, EXTCLK 7/	$t_{f(EXTCLK)}$		$F = F_{max}$, x0.5 and x1 modes	25°C, -40°C to 100°C	01		1	ns
				25°C, -55°C to 125°C	02		1	
			$F < F_{max}$	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Pulse duration, EXTCLK low 7/	$t_{w(EXTCLKL)}$		x5 mode	25°C, -40°C to 100°C	01	21		ns
				25°C, -55°C to 125°C	02	21		
			x1 mode	25°C, -40°C to 100°C	01	5.5		
				25°C, -55°C to 125°C	02	5.5		
			x0.5 mode	25°C, -40°C to 100°C	01	4		
				25°C, -55°C to 125°C	02	4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing requirements for EXTCLK, all modes - Continued								
Pulse duration, EXTCLK high 7/	$t_{w(EXTCLKH)}$	See figure 4	x5 mode	25°C, -40°C to 100°C	01	21		ns
				25°C, -55°C to 125°C	02	21		
			x1 mode	25°C, -40°C to 100°C	01	5.5		
				25°C, -55°C to 125°C	02	5.5		
			x0.5 mode	25°C, -40°C to 100°C	01	4		
				25°C, -55°C to 125°C	02	4		
Duty cycle, EXTCLK $[t_{w(EXTCLKH)}/t_{c(H)}]$	$t_{dc(EXTCLK)}$		x5 PLL mode 7/	25°C, -40°C to 100°C	01	40	60	%
				25°C, -55°C to 125°C	02	40	60	
			x1 and x0.5 modes, $F = F_{max}$	25°C, -40°C to 100°C	01	45	55	
				25°C, -55°C to 125°C	02	45	55	
			x1 and x0.5 modes, F = 0 Hz 7/	25°C, -40°C to 100°C	01	0	100	
				25°C, -55°C to 125°C	02	0	100	
Cycle time, EXTCLK	$t_{c(EXTCLK)}$		x5 mode 7/	25°C, -40°C to 100°C	01	66.7	200	ns
				25°C, -55°C to 125°C	02	66.7	200	
			x1 mode	25°C, -40°C to 100°C	01	13.3		
				25°C, -55°C to 125°C	02	13.3		
			x0.5 mode 7/	25°C, -40°C to 100°C	01	10		
				25°C, -55°C to 125°C	02	10		
Frequency range, $1/t_{c(EXTCLK)}$	F_{ext}		x5 mode 7/	25°C, -40°C to 100°C	01	5	15	MHz
				25°C, -55°C to 125°C	02	5	15	
			x1 mode	25°C, -40°C to 100°C	01	0	75	
				25°C, -55°C to 125°C	02	0	75	
			x0.5 mode 7/	25°C, -40°C to 100°C	01	0	100	
				25°C, -55°C to 125°C	02	0	100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Switching characteristics for EXTCLK over recommended operating conditions, all modes								
Mid-level, used to measure duty cycle	V_{mid}	See figure 4		25°C, -40°C to 100°C	01	$0.5DV_{DD}$ typical		V
				25°C, -55°C to 125°C	02	$0.5DV_{DD}$ typical		
Delay time, EXTCLK to H1 and H3 7/	$t_{d(EXTCLK-H)}$		x1 mode	25°C, -40°C to 100°C	01	2	7	ns
				25°C, -55°C to 125°C	02	2	7	
			x0.5 mode	25°C, -40°C to 100°C	01	2	7	
				25°C, -55°C to 125°C	02	2	7	
Rise time, H1 and H3 7/	$t_{r(H)}$			25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	
Fall time, H1 and H3 7/	$t_{f(H)}$			25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	
Delay time, from H1 low to H3 high or from H3 low to H1 high 7/	$t_{d(HL-HH)}$			25°C, -40°C to 100°C	01	-1.5	2	ns
				25°C, -55°C to 125°C	02	-1.5	2	
Cycle time, H1 and H3	$t_{c(H)}$		x5 PLL mode	25°C, -40°C to 100°C	01	1/(5fext) typical		ns
				25°C, -55°C to 125°C	02	1/(5fext) typical		
			x1 mode	25°C, -40°C to 100°C	01	1/fext typical		
				25°C, -55°C to 125°C	02	1/fext typical		
			x0.5 mode	25°C, -40°C to 100°C	01	2/fext typical		
				25°C, -55°C to 125°C	02	2/fext typical		
Timing requirements for memory read/write 11/								
Setup time, data before H1 low (read) 7/	$t_{su(D-H1L)R}$	See figure 4		25°C, -40°C to 100°C	01	5		ns
				25°C, -55°C to 125°C	02	5		
Hold time, data after H1 low (read) 7/	$t_{h(H1L-D)R}$			25°C, -40°C to 100°C	01	-1		ns
				25°C, -55°C to 125°C	02	-1		
Setup time, $\overline{RDY}$ before H1 high	$t_{su(RDY-H1H)}$			25°C, -40°C to 100°C	01	5		ns
				25°C, -55°C to 125°C	02	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing requirements for memory read/write - Continued 11/								
Hold time, $\overline{RDY}$ after H1 high 7/	$t_{h(H1H-RDY)}$	See figure 4		25°C, -40°C to 100°C	01	-1		ns
				25°C, -55°C to 125°C	02	-1		
Delay time, address valid to $\overline{RDY}$ 7/	$t_{d(A-RDY)}$			25°C, -40°C to 100°C	01		P-7 10/	ns
				25°C, -55°C to 125°C	02		P-6 10/	
Valid time, data valid after address $\overline{PAGEx}$, or $\overline{STRB}$ valid 7/	$t_{v(A-D)}$	See figure 4	0 wait state, C_L = 30 pF	25°C, -40°C to 100°C	01		9	ns
				25°C, -55°C to 125°C	02		6	
			1 wait state	25°C, -40°C to 100°C	01		$t_{c(H)}$+9	
				25°C, -55°C to 125°C	02		$t_{c(H)}$+6	
Switching characteristics over recommended operating conditions for memory read/write 11/								
Delay time, H1 low to $\overline{STRB}$ low	$t_{d(H1L-SL)}$	See figure 4		25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Delay time, H1 low to $\overline{STRB}$ high	$t_{d(H1L-SH)}$			25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Delay time, H1 high to R/$\overline{W}$ low (write)	$t_{d(H1H-RWL)W}$			25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Delay time, H1 low to address valid	$t_{d(H1L-A)}$			25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Delay time, H1 high to R/$\overline{W}$ high (write)	$t_{d(H1H-RWH)W}$			25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for memory read/write - Continued 11/							
Delay time, H1 high to address valid on back-to-back write cycles (write)	$t_{d(H1H-A)W}$	See figure 4	25°C, -40°C to 100°C	01	-1 7/	4 7/	ns
			25°C, -55°C to 125°C	02	-1 7/	3 7/	
Valid time, data after H1 low (write)	$t_{v(H1L-D)W}$		25°C, -40°C to 100°C	01		6	ns
			25°C, -55°C to 125°C	02		5	
Hold time, data after H1 high (write)	$t_{h(H1H-D)W}$		25°C, -40°C to 100°C	01	0 7/	5	ns
			25°C, -55°C to 125°C	02	0 7/	5	
Timing requirements for XF0 and XF1 when executing LDFI or LDII							
Setup time, XF1 before H1 low 7/	$t_{su(XF1-H1L)}$	See figure 4	25°C, -40°C to 100°C	01	5		ns
			25°C, -55°C to 125°C	02	4		
Hold time, XF1 after H1 low 7/	$t_{h(H1L-XF1)}$		25°C, -40°C to 100°C	01	0		ns
			25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for XF0 and XF1 when excecuting LDFI or LDII							
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Switching characteristics over recommended operating conditions for XF0 when excecuting STFI or STII							
Delay time, H3 high to XF0 high 13/	$t_{d(H3H-XF0H)}$	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for XF0 and XF1 when executing SIGI							
Setup time, XF1 before H1 low 7/	$t_{su(XF1-H1L)}$	See figure 4	25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Hold time, XF1 after H1 low 7/	$t_{h(H1L-XF1)}$		25°C, -40°C to 100°C	01		0	ns
			25°C, -55°C to 125°C	02		0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for XF0 and XF1 when excecuting SIGI							
Delay time, H3 high to XF0 low	$t_{d(H3H-XF0L)}$	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H3 high to XF0 high	$t_{d(H3H-XF0H)}$		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Switching characteristics over recommended operating conditions for loading the XF register when configured as an output pin							
Valid time, XFx after H3 high	$t_{v(H3H-XF)}$	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for changing XFx from output to input mode							
Setup time, XFx before H1 low	$t_{su(XF-H1L)}$	See figure 4	25°C, -40°C to 100°C	01	5		ns
			25°C, -55°C to 125°C	02	4		
Hold time, XFx after H1 low	$t_{h(H1L-XF)}$		25°C, -40°C to 100°C	01	0		ns
			25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for changing XFx from output to input mode							
Disable time, XFx after H3 high 7/	$t_{dis(H3H-XF)}$	See figure 4	25°C, -40°C to 100°C	01		6	ns
			25°C, -55°C to 125°C	02		5	
Switching characteristics over recommended operating conditions for changing XFx from input to output mode							
Delay time, H3 high to XFx switching from input to output	$t_{d(H3H-XF)}$	See figure 4	25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Timing requirements for $\overline{\text{RESET}}$							
Setup time, $\overline{\text{RESET}}$ before EXTCLK low 7/	$t_{su(RESET-EXTCLKL)}$	See figure 4	25°C, -40°C to 100°C	01	6	P-7 14/	ns
			25°C, -55°C to 125°C	02	5	P-7 14/	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	$t_{su(RESETH-H1L)}$		25°C, -40°C to 100°C	01	6		ns
			25°C, -55°C to 125°C	02	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for $\overline{\text{RESET}}$							
Delay time, EXTCLK high to H1 high 7/	$t_{d(EXTCLKH-H1H)}$	See figure 4	25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H1 low 7/	$t_{d(EXTCLKH-H1L)}$		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H3 low 7/	$t_{d(EXTCLKH-H3L)}$		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Delay time, EXTCLK high to H3 high 7/	$t_{d(EXTCLKH-H3H)}$		25°C, -40°C to 100°C	01	2	7	ns
			25°C, -55°C to 125°C	02	2	7	
Disable time, data (high impedance) from H1 high 7/ 15/	$t_{dis(H1H-DZ)}$		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	
Disable time, address (high impedance) from H3 high 7/	$t_{dis(H3H-AZ)}$		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	
Delay time, H3 high to control signals high 7/	$t_{d(H3H-CONTROLH)}$		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H1 high to R/$\overline{W}$ high 7/	$t_{d(H1H-RWH)}$		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Delay time, H1 high to $\overline{\text{IACK}}$ high 7/	$t_{d(H1H-IACKH)}$		25°C, -40°C to 100°C	01		4	ns
			25°C, -55°C to 125°C	02		3	
Disable time, asynchronous reset signals disabled (high impedance) from $\overline{\text{RESET}}$ low 7/ 16/	$t_{dis(RESETL-ASYNCH)}$		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing requirements for $\overline{INT3}$ - $\overline{INT0}$ response								
Setup time, $\overline{INT3}$ - $\overline{INT0}$ before H1 low 7/	$t_{su(INT-H1L)}$	See figure 4		25°C, -40°C to 100°C	01	5		ns
				25°C, -55°C to 125°C	02	4		
Hold time, $\overline{INT3}$ - $\overline{INT0}$ after H1 low	$t_{h(H1L-INT)}$			25°C, -40°C to 100°C	01		0	ns
				25°C, -55°C to 125°C	02		0	
Pulse duration, interrupt to ensure only one interrupt 7/ 17/	$t_{w(INT)}$			25°C, -40°C to 100°C	01	P+5	2P-5	ns
				25°C, -55°C to 125°C	02	P+5	2P-5	
Switching characteristics over recommended operating conditions for $\overline{IACK}$								
Delay time, H1 high to $\overline{IACK}$ low	$t_{d(H1H-IACKL)}$	See figure 4		25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Delay time, H1 high to $\overline{IACK}$ high	$t_{d(H1H-IACKH)}$			25°C, -40°C to 100°C	01	-1 7/	4	ns
				25°C, -55°C to 125°C	02	-1 7/	3	
Timimg requirements for serial port parameters								
Cycle time, CLKX/R 7/	$t_{c(SCK)}$	See figure 4	CLKX/R ext	25°C, -40°C to 100°C	01	$t_{c(H)}$x2.6		ns
				25°C, -55°C to 125°C	02	$t_{c(H)}$x2.6		
			CLKX/R int	25°C, -40°C to 100°C	01	$t_{c(H)}$x4 18/	$t_{c(H)}x2^{16}$	
				25°C, -55°C to 125°C	02	$t_{c(H)}$x4 18/	$t_{c(H)}x2^{16}$	
Pulse duration, CLKX/R high/low	$t_{w(SCK)}$		CLKX/R ext	25°C, -40°C to 100°C	01	$t_{c(H)}$+5		ns
				25°C, -55°C to 125°C	02	$t_{c(H)}$+5		
			CLKX/R int 7/	25°C, -40°C to 100°C	01	$[t_{c(SCK)}/2]$-4	$[t_{c(SCK)}/2]$+4	
				25°C, -55°C to 125°C	02	$[t_{c(SCK)}/2]$-4	$[t_{c(SCK)}/2]$+4	
Rise time, CLKX/R 7/	$t_{r(SCK)}$	See figure 4		25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	
Fall time, CLKX/R 7/	$t_{f(SCK)}$			25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timimg requirements for serial port parameters - Continued								
Setup time, DR before CLKR low 7/	$t_{su(DR-CLKRL)}$	See figure 4	CLKR ext	25°C, -40°C to 100°C	01	4		ns
				25°C, -55°C to 125°C	02	4		
			CLKR int	25°C, -40°C to 100°C	01	5		
				25°C, -55°C to 125°C	02	5		
Hold time, DR after CLKR low 7/	$t_{h(CLKRL-DR)}$		CLKR ext	25°C, -40°C to 100°C	01	3		ns
				25°C, -55°C to 125°C	02	3		
			CLKR int	25°C, -40°C to 100°C	01	0		
				25°C, -55°C to 125°C	02	0		
Setup time, FSR before CLKR low 7/	$t_{su(FSR-CLKRL)}$		CLKR ext	25°C, -40°C to 100°C	01	4		ns
				25°C, -55°C to 125°C	02	4		
			CLKR int	25°C, -40°C to 100°C	01	5		
				25°C, -55°C to 125°C	02	5		
Hold time, FSX/R input after CLKX/R low 7/	$t_{h(SCKL-FS)}$		CLKX/R ext	25°C, -40°C to 100°C	01	3		ns
				25°C, -55°C to 125°C	02	3		
			CLKX/R int	25°C, -40°C to 100°C	01	0		
				25°C, -55°C to 125°C	02	0		
Setup time, external FSX before CLKX 7/	$t_{su(FSX-CLKX)}$		CLKX ext	25°C, -40°C to 100°C	01	$-[t_{c(H)}-6]$	$[t_{c(SCK)}/2]-6$	ns
				25°C, -55°C to 125°C	02	$-[t_{c(H)}-6]$	$[t_{c(SCK)}/2]-6$	
			CLKX int	25°C, -40°C to 100°C	01	$-[t_{c(H)}-10]$	$t_{c(SCK)}/2$	
				25°C, -55°C to 125°C	02	$-[t_{c(H)}-10]$	$t_{c(SCK)}/2$	
Switching characteristics over recommended operating conditions for serial port parameters								
Delay time, H1 high to internal CLKX/R 7/	$t_{d(H1H-SCK)}$	See figure 4		25°C, -40°C to 100°C	01		4	ns
				25°C, -55°C to 125°C	02		4	
Delay time, CLKX to DX valid	$t_{d(CLKX-DX)}$	See figure 4	CLKX ext	25°C, -40°C to 100°C	01		6	ns
				25°C, -55°C to 125°C	02		6	
			CLKX int 7/	25°C, -40°C to 100°C	01		5	
				25°C, -55°C to 125°C	02		5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Switching characteristics over recommended operating conditions for serial port parameters – Continued								
Delay time, CLKX to internal FSX high/low	$t_{d(CLKX-FSX)}$	See figure 4	CLKX ext	25°C, -40°C to 100°C	01		5	ns
				25°C, -55°C to 125°C	02		5	
			CLKX int 7/	25°C, -40°C to 100°C	01		4	
				25°C, -55°C to 125°C	02		4	
Delay time, CLKX to first DX bit, FSX precedes CLKX high	$t_{d(CLKX-DX)V}$		CLKX ext	25°C, -40°C to 100°C	01		4	ns
				25°C, -55°C to 125°C	02		4	
			CLKX int 7/	25°C, -40°C to 100°C	01		5	
				25°C, -55°C to 125°C	02		5	
Delay time, FSX to first DX bit, CLKX precedes FSX	$t_{d(FSX-DX)V}$	See figure 4		25°C, -40°C to 100°C	01		6	ns
				25°C, -55°C to 125°C	02		6	
Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CLKX-DXZ)}$			25°C, -40°C to 100°C	01		6	ns
				25°C, -55°C to 125°C	02		6	
Timing requirements for $\overline{\text{HOLD}}$ / $\overline{\text{HOLDA}}$								
Setup time, $\overline{\text{HOLD}}$ before H1 low	$t_{su(HOLD-H1L)}$	See figure 4		25°C, -40°C to 100°C	01	3		ns
				25°C, -55°C to 125°C	02	4		
Pulse duration, $\overline{\text{HOLD}}$ low 7/	$t_{w(HOLD)}$			25°C, -40°C to 100°C	01	$3t_{c(H)}$		ns
				25°C, -55°C to 125°C	02	$3t_{c(H)}$		
Switching characteristics over recommended operating conditions for $\overline{\text{HOLD}}$ / $\overline{\text{HOLDA}}$								
Valid time, $\overline{\text{HOLDA}}$ after H1 low 7/	$t_{v(H1L-HOLDA)}$	See figure 4		25°C, -40°C to 100°C	01	-1	4	ns
				25°C, -55°C to 125°C	02	-1	3	
Pulse duration, $\overline{\text{HOLDA}}$ low 7/	$t_{w(HOLDA)}$			25°C, -40°C to 100°C	01	$2t_{c(H)}$-4		ns
				25°C, -55°C to 125°C	02	$2t_{c(H)}$-4		
Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	$t_{d(H1L-SH)H}$			25°C, -40°C to 100°C	01	-1	4	ns
				25°C, -55°C to 125°C	02	-1	3	
Disable time, $\overline{\text{STRB}}$ to the high-impedance state from H1 low	$t_{dis(H1L-S)}$			25°C, -40°C to 100°C	01		5	ns
				25°C, -55°C to 125°C	02		4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified	Temperature, T_C	Device type	Limits		Unit
					Min	Max	
Switching characteristics over recommended operating conditions for $\overline{\text{HOLD}}$ / $\overline{\text{HOLDA}}$ - Continued							
Enable time, $\overline{\text{STRB}}$ enabled (active) from H1 low	$t_{en(H1L-S)}$	See figure 4	25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Disable time, R/$\overline{\text{W}}$ to the high-impedance state from H1 low 7/	$t_{dis(H1L-RW)}$		25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		5	
Enable time, R/$\overline{\text{W}}$ enabled (active) from H1 low	$t_{en(H1L-RW)}$		25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Disable time, address to the high-impedance state from H1 low 7/	$t_{dis(H1L-A)}$		25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Enable time, address enabled (valid) from H1 low	$t_{en(H1L-A)}$		25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		5	
Disable time, data to the high-impedance state from H1 high 7/	$t_{dis(H1H-D)}$		25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Timing requirements for peripheral pin general-purpose I/O 19/							
Setup time, general-purpose input before H1 low 7/	$t_{su(GPIO-H1L)}$	See figure 4	25°C, -40°C to 100°C	01	4		ns
			25°C, -55°C to 125°C	02	3		
Hold time, general-purpose input after H1 low 7/	$t_{h(H1L-GPIO)}$		25°C, -40°C to 100°C	01	0		ns
			25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for peripheral pin general-purpose I/O 19/							
Delay time, H1 high to general-purpose output	$t_{d(H1H-GPIO)}$	See figure 4	25°C, -40°C to 100°C	01		5	ns
			25°C, -55°C to 125°C	02		4	
Disable time, general-purpose output from H1 high	$t_{dis(H1H)}$		25°C, -40°C to 100°C	01		7	ns
			25°C, -55°C to 125°C	02		5	
Timing requirements for timer pin							
Setup time, TCLK external before H1 low 7/ 20/	$t_{su(TCLK-H1L)}$	See figure 4	25°C, -40°C to 100°C	01	4		ns
			25°C, -55°C to 125°C	02	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $3.0\ V \le DV_{DD} \le 3.6\ V$ $1.71\ V \le CV_{DD} \le 1.89\ V$ unless otherwise specified		Temperature, T_C	Device type	Limits		Unit
						Min	Max	
Timing requirements for timer pin - Continued								
Hold time, TCLK external after H1 low 20/	$t_{h(H1L-TCLK)}$	See figure 4		25°C, -40°C to 100°C	01	0		ns
				25°C, -55°C to 125°C	02	0		
Switching characteristics over recommended operating conditions for timer pin								
Delay time, H1 high to TCLK internal valid	$t_{d(H1H-TCLK)}$	See figure 4		25°C, -40°C to 100°C	01		4	ns
				25°C, -55°C to 125°C	02		3	
Cycle time, TCLK 7/ 21/	$t_{c(TCLK)}$		TCLK ext	25°C, -40°C to 100°C	01	$t_{c(H)}x2.6$		ns
				25°C, -55°C to 125°C	02	$t_{c(H)}x2.6$		
			TCLK int	25°C, -40°C to 100°C	01	$t_{c(H)}x2$	$t_{c(H)}x2^{32}$	
				25°C, -55°C to 125°C	02	$t_{c(H)}x2$	$t_{c(H)}x2^{32}$	
Pulse duration, TCLK 7/ 21/	$t_{w(TCLK)}$		TCLK ext	25°C, -40°C to 100°C	01	$t_{c(H)}+6$		ns
				25°C, -55°C to 125°C	02	$t_{c(H)}+5$		
			TCLK int	25°C, -40°C to 100°C	01	$[t_{c(TCLK)}/2]-4$	$[t_{c(TCLK)}/2]+4$	
				25°C, -55°C to 125°C	02	$[t_{c(TCLK)}/2]-4$	$[t_{c(TCLK)}/2]+4$	
Switching characteristics over recommended operating conditions for $\overline{SHZ}$								
Disable time, $\overline{SHZ}$ low to all outputs, I/O pins disabled (high impedance) 7/	$t_{dis(SHZ)}$	See figure 4		25°C, -40°C to 100°C	01	0	8	ns
				25°C, -55°C to 125°C	02	0	8	
Timing for test access port								
Setup time, TMS/TDI to TCK high 7/	$t_{su(TMH-TCKH)}$	See figure 4		25°C, -40°C to 100°C	01	5		ns
				25°C, -55°C to 125°C	02	5		
Hold time, TMS/TDI from TCK high 7/	$t_{h(TCKH-TMH)}$			25°C, -40°C to 100°C	01	5		ns
				25°C, -55°C to 125°C	02	5		
Delay time, TCK low to TDO valid 7/	$t_{d(TCKL-TDOV)}$			25°C, -40°C to 100°C	01	0	10	ns
				25°C, -55°C to 125°C	02	0	10	
Rise time, TCK 7/	$t_{r(TCK)}$			25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	
Fall time, TCK 7/	$t_{f(TCK)}$			25°C, -40°C to 100°C	01		3	ns
				25°C, -55°C to 125°C	02		3	

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ All voltage values are with respect to V_{SS}.

2/ For test conditions shown as Min or Max, use the appropriate value specified in section 1.4, herein.

3/ Pins with internal pullup devices: TDI, TCK, and TMS. Pins with internal pulldown devices: $\overline{\text{TRST}}$.

4/ Pins D0 – D31 include internal bus keepers that maintain valid logic levels when the bus is not driven.

5/ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible.

6/ f_x is the PLL output clock frequency.

7/ Not production tested.

8/ Duty cycle is defined as $100xt_1/(t_1+t_2)\%$.

9/ This circuit is intended for series resonant fundamental mode operation.

10/ Signal amplitude is dependent on the crystal and load used.

11/ These timings assume a similar loading of 30 pF on all pins.

12/ $P = t_{c(H)}/2$ (when duty cycle equals 50%).

13/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store is not driven until the store can execute.

14/ $P = t_{c(EXTCLK)}$.

15/ High impedance for data bus is limited to nominal bus keeper Z_{OUT} = 15 kΩ.

16/ Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

17/ $P = t_{c(H)}$.

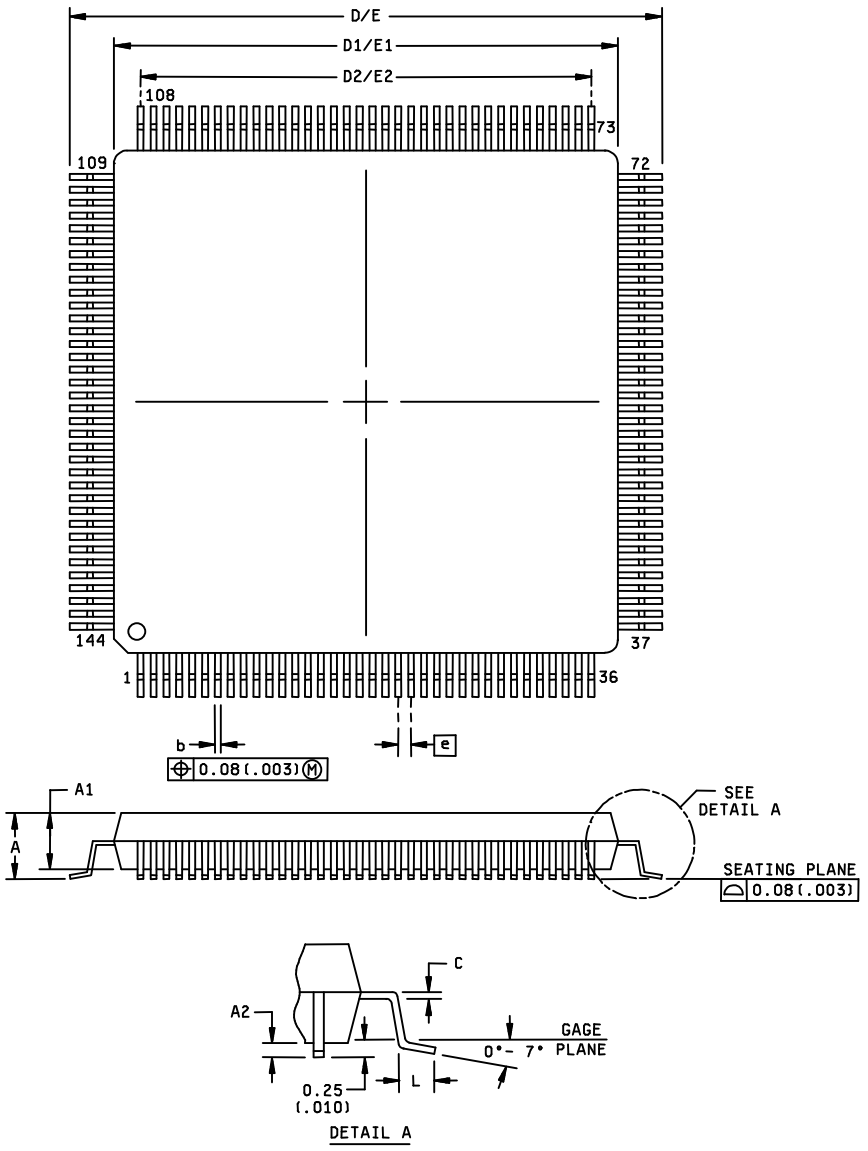
18/ A cycle time of $t_{c(H)}x2$ is possible when the device is operated at lower CPU frequencies.

19/ Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.

20/ These requirements are applicable for a synchronous input clock.

21/ These requirements are applicable for an asynchronous input clock.

Case X



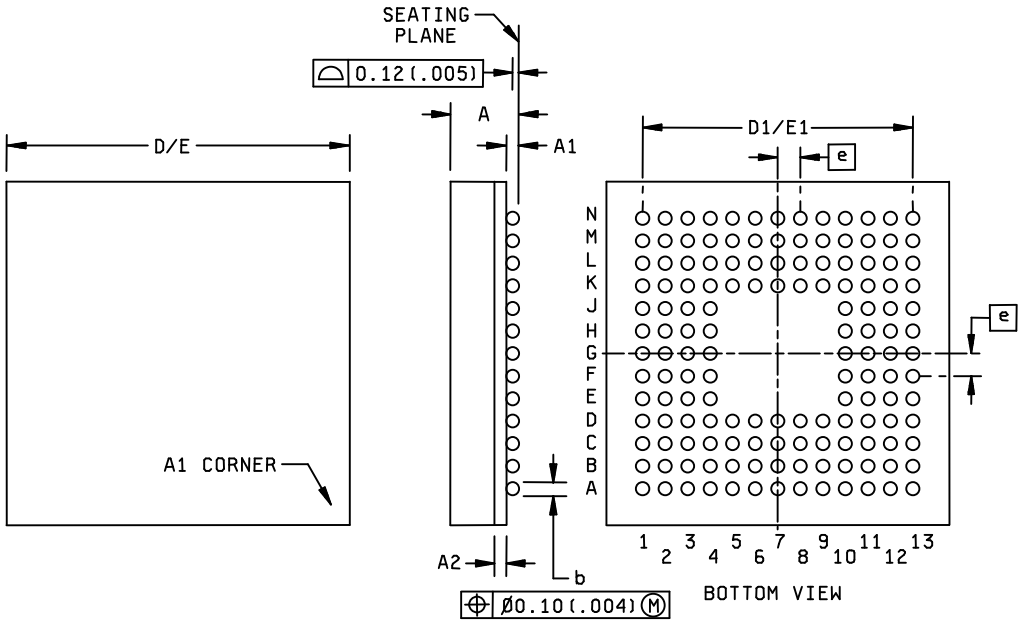
NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
4. Fall within JEDEC MS-026.

FIGURE 1. Case outlines.

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		1.60
A1	1.35	1.45
A2	0.05	
b	0.17	0.27
c	0.13 NOM	
D/E	21.80	22.20
D1/E1	19.80	20.20
D2/E2	17.50 TYP	
e	0.59 BSC	
L	0.45	0.75

FIGURE 1. Case outlines - Continued.

Case Y



NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		2.40
A1	0.35	0.50
A2	0.34	0.56
b	0.45	0.55
D/E	11.85	12.15
D1/E1	9.60 TYP	
e	0.80 BSC	

FIGURE 1. Case outlines - Continued.

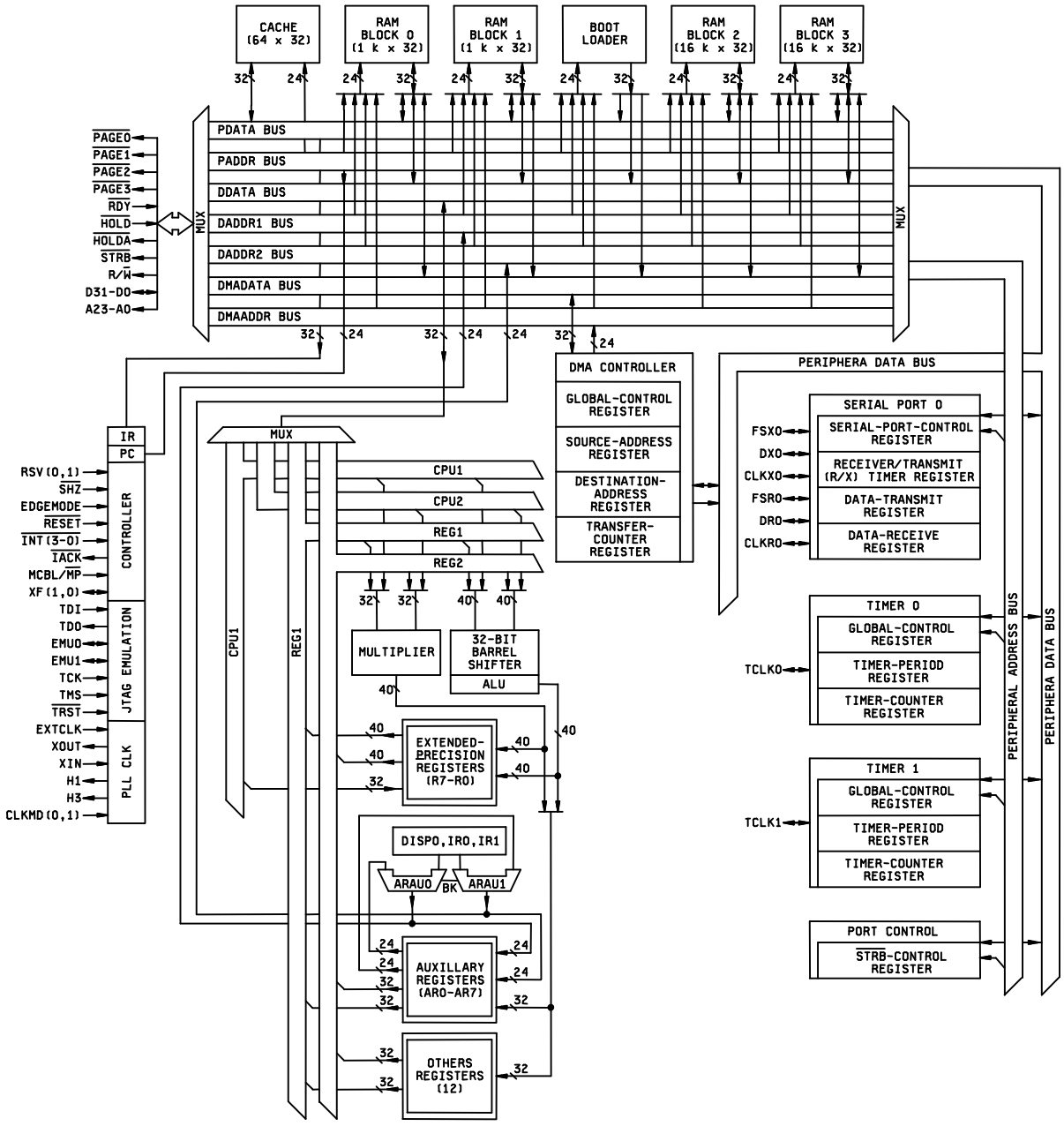


FIGURE 2. Functional block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03610
		REV	PAGE 24

Case outline	X				
Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
1	A20	25	V_{SS}	49	V_{SS}
2	V_{SS}	26	A3	50	D31
3	A19	27	A2	51	D30
4	A18	28	CV_{DD}	52	D29
5	A17	29	A1	53	DV_{DD}
6	DV_{DD}	30	A0	54	D28
7	A16	31	DV_{DD}	55	D27
8	A15	32	$\overline{PAGE3}$	56	V_{SS}
9	V_{SS}	33	$\overline{PAGE2}$	57	D26
10	A14	34	V_{SS}	58	D25
11	A13	35	$\overline{PAGE1}$	59	D24
12	CV_{DD}	36	$\overline{PAGE0}$	60	DV_{DD}
13	A12	37	DV_{DD}	61	D23
14	A11	38	H1	62	D22
15	DV_{DD}	39	H3	63	V_{SS}
16	A10	40	V_{SS}	64	D21
17	A9	41	$\overline{STRB}$	65	D20
18	V_{SS}	42	R/$\overline{W}$	66	CV_{DD}
19	A8	43	DV_{DD}	67	D19
20	A7	44	$\overline{IACK}$	68	D18
21	A6	45	$\overline{RDY}$	69	DV_{DD}
22	A5	46	CV_{DD}	70	D17
23	DV_{DD}	47	$\overline{HOLD}$	71	D16
24	A4	48	$\overline{HOLDA}$	72	V_{SS}

See footnote at end of table.

FIGURE 3. Terminal connections.

Case outline	X				
Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
73	D15	97	V_{SS}	121	$\overline{INT1}$
74	D14	98	TCK	122	$\overline{INT0}$
75	D13	99	TDO	123	CV_{DD}
76	D12	100	TDI	124	EDGEMODE
77	DV_{DD}	101	CV_{DD}	125	MCBL/$\overline{MP}$
78	D11	102	TMS	126	V_{SS}
79	D10	103	$\overline{TRST}$	127	$\overline{RESET}$
80	V_{SS}	104	DR0	128	$\overline{SHZ}$
81	D9	105	V_{SS}	129	DV_{DD}
82	D8	106	FSR0	130	EXTCLK
83	CV_{DD}	107	CLKR0	131	$PLLV_{DD}$ 2/
84	D7	108	DV_{DD}	132	XOUT
85	D6	109	CLKX0	133	XIN
86	DV_{DD}	110	FSX0	134	$PLLV_{SS}$ 2/
87	D5	111	DX0	135	CLKMD1
88	D4	112	V_{SS}	136	CLKMD0
89	V_{SS}	113	TCLK1	137	CV_{DD}
90	D3	114	TCLK0	138	RSV1
91	D2	115	DV_{DD}	139	RSV0
92	D1	116	XF1	140	V_{SS}
93	D0	117	XF0	141	A23
94	DV_{DD}	118	V_{SS}	142	A22
95	EMU1	119	$\overline{INT3}$	143	DV_{DD}
96	EMU0	120	$\overline{INT2}$	144	A21

1/ DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.
2/ $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

FIGURE 3. Terminal connections – Continued.

Case outline	Y				
Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
A1	DV_{DD}	B12	DV_{DD}	D10	FSX
A2	A22	B13	CLKR0	D11	DR0
A3	CV_{DD}	C1	A16	D12	CV_{DD}
A4	$PLLV_{SS}$ 2/	C2	A17	D13	TDO
A5	$PLLV_{DD}$ 2/	C3	A19	E1	A13
A6	DV_{DD}	C4	V_{SS}	E2	A14
A7	EDGEMODE	C5	CLKMD0	E3	CV_{DD}
A8	CV_{DD}	C6	EXTCLK	E4	A15
A9	$\overline{INT3}$	C7	V_{SS}	E10	TMS
A10	DV_{DD}	C8	$\overline{INT0}$	E11	TDI
A11	TCLK1	C9	V_{SS}	E12	EMU1
A12	DX	C10	TCLK0	E13	V_{SS}
A13	V_{SS}	C11	V_{SS}	F1	DV_{DD}
B1	V_{SS}	C12	FSR0	F2	A12
B2	A20	C13	$\overline{TRST}$	F3	A10
B3	A23	D1	V_{SS}	F4	A11
B4	RSV0	D2	DV_{DD}	F10	TCK
B5	CLKMD1	D3	A18	F11	DV_{DD}
B6	XIN	D4	A21	F12	EMU0
B7	$\overline{RESET}$	D5	RSV1	F13	D2
B8	MCBL/$\overline{MP}$	D6	XOUT	G1	A8
B9	$\overline{INT1}$	D7	$\overline{SHZ}$	G2	A9
B10	XF0	D8	$\overline{INT2}$	G3	V_{SS}
B11	CLKX0	D9	XF1	G4	A7

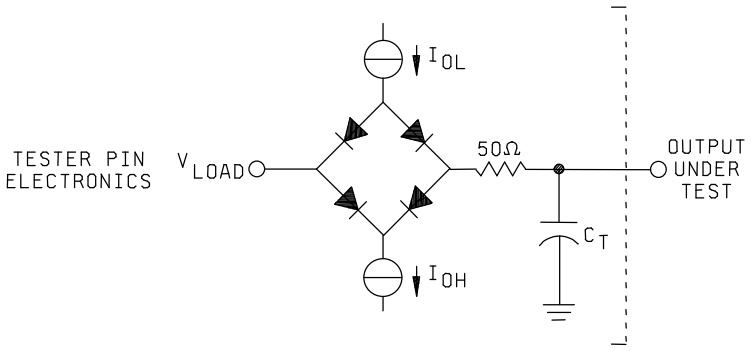
See footnotes at end of table.

FIGURE 3. Terminal connections - Continued.

Case outline	Y				
Pin number	Pin name 1/	Pin number	Pin name 1/	Pin number	Pin name 1/
G10	D1	K5	$\overline{\text{HOLDA}}$	M3	V_{SS}
G11	D3	K6	D31	M4	$\overline{\text{STRB}}$
G12	D0	K7	D28	M5	$\overline{\text{RDY}}$
G13	V_{SS}	K8	D22	M6	V_{SS}
H1	A6	K9	D18	M7	D27
H2	DV_{DD}	K10	D12	M8	DV_{DD}
H3	A5	K11	V_{SS}	M9	D24
H4	A4	K12	D11	M10	D21
H10	D4	K13	D10	M11	D20
H11	DV_{DD}	L1	$\overline{\text{PAGE2}}$	M12	D16
H12	D6	L2	V_{SS}	M13	D13
H13	D5	L3	H1	N1	DV_{DD}
J1	V_{SS}	L4	R/$\overline{\text{W}}$	N2	H3
J2	A0	L5	CV_{DD}	N3	$\overline{\text{PAGE1}}$
J3	CV_{DD}	L6	D29	N4	DV_{DD}
J4	A3	L7	V_{SS}	N5	$\overline{\text{HOLD}}$
J10	D7	L8	D25	N6	D30
J11	D8	L9	CV_{DD}	N7	DV_{DD}
J12	D9	L10	D17	N8	D26
J13	CV_{DD}	L11	D14	N9	D23
K1	A2	L12	D15	N10	V_{SS}
K2	A1	L13	DV_{DD}	N11	D19
K3	$\overline{\text{PAGE3}}$	M1	DV_{DD}	N12	DV_{DD}
K4	$\overline{\text{IACK}}$	M2	$\overline{\text{PAGE0}}$	N13	V_{SS}

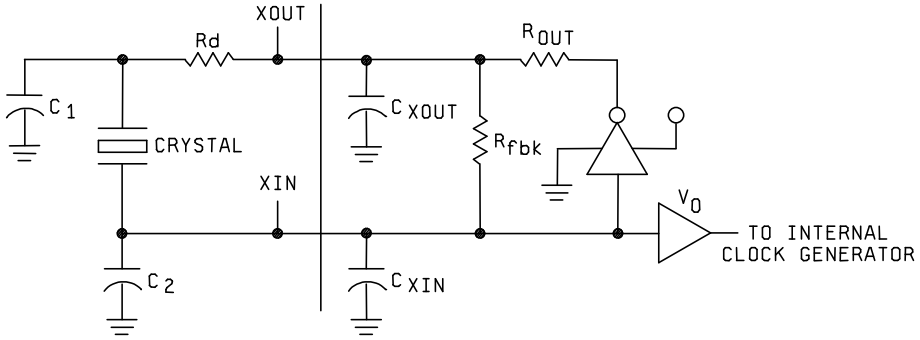
1/ DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.
2/ $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

FIGURE 3. Terminal connections – Continued.



TEST CIRCUIT

NOTES: I_{OL} = 4.0 mA (all outputs) for dc levels test.
I_{OL} and I_{OH} are adjusted during ac timing analysis to achieve an ac termination of 50Ω.
$V_{LOAD} = DV_{DD}/2$.
C_T = 40 pF, typical load-circuit capacitance.



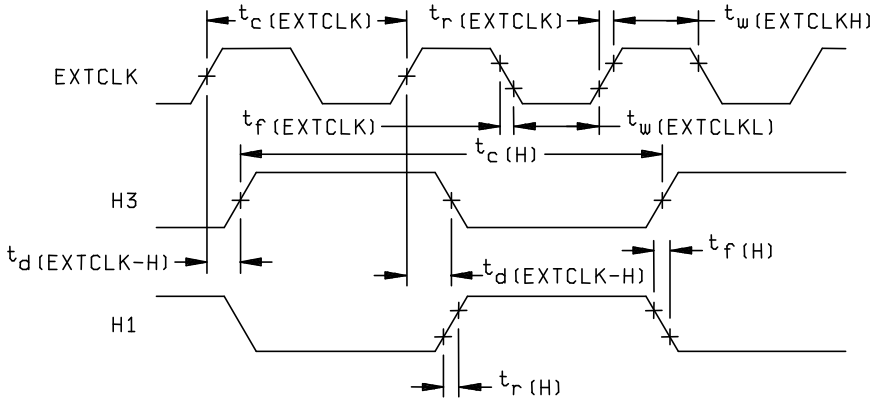
ON-CHIP OSCILLATOR CIRCUIT

Frequency (MHz)	Rd (Ω)	C1 (pF)	C2 (pF)	CL (pF) 1/	RL (Ω) 1/
2	4700	18	18	12	200
5	2200	18	18	12	60
10	470	15	15	12	30
15	0	15	12	12	25
20	0	9	9	10	25

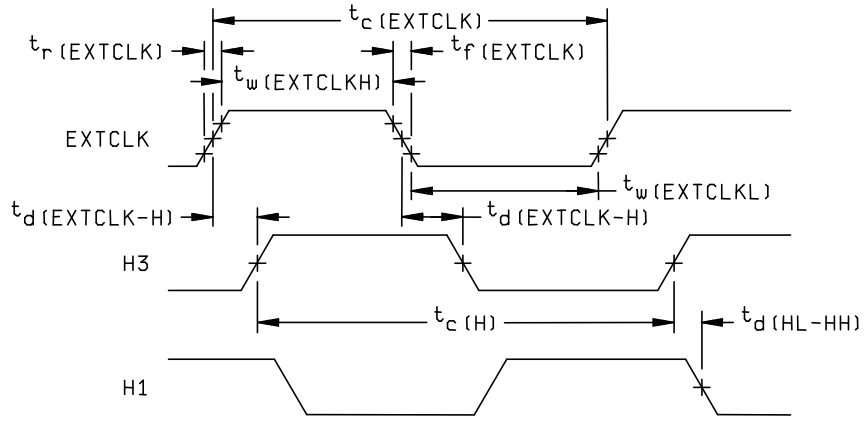
1/ CL and RL are typical internal series load capacitance and resistance of the crystal.

TYPICAL CRYSTAL CIRCUIT LOADING

FIGURE 4. Test circuit and timing waveforms.



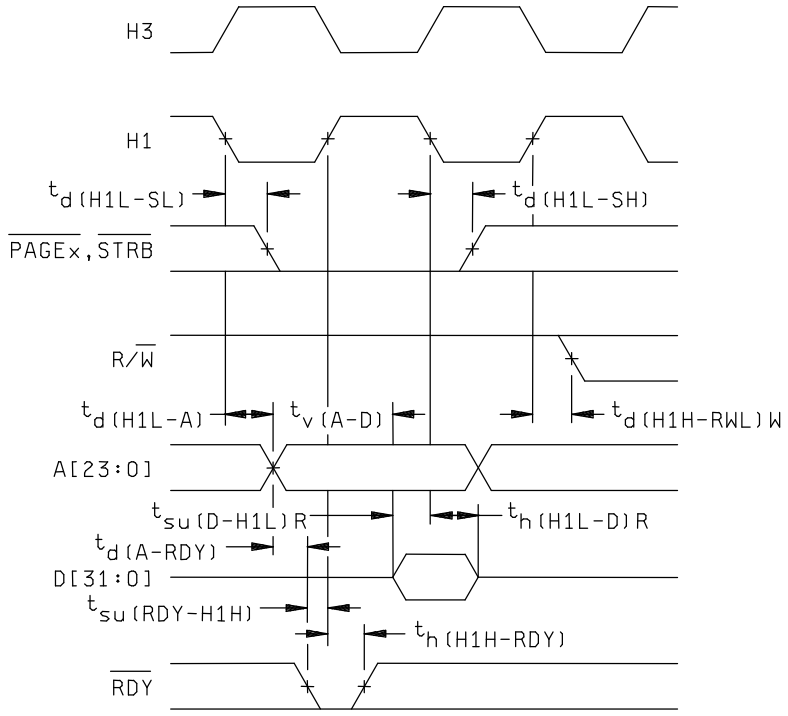
DIVIDE-BY-TWO MODE



DIVIDE-BY-ONE MODE

NOTE: EXTCLK is held low.

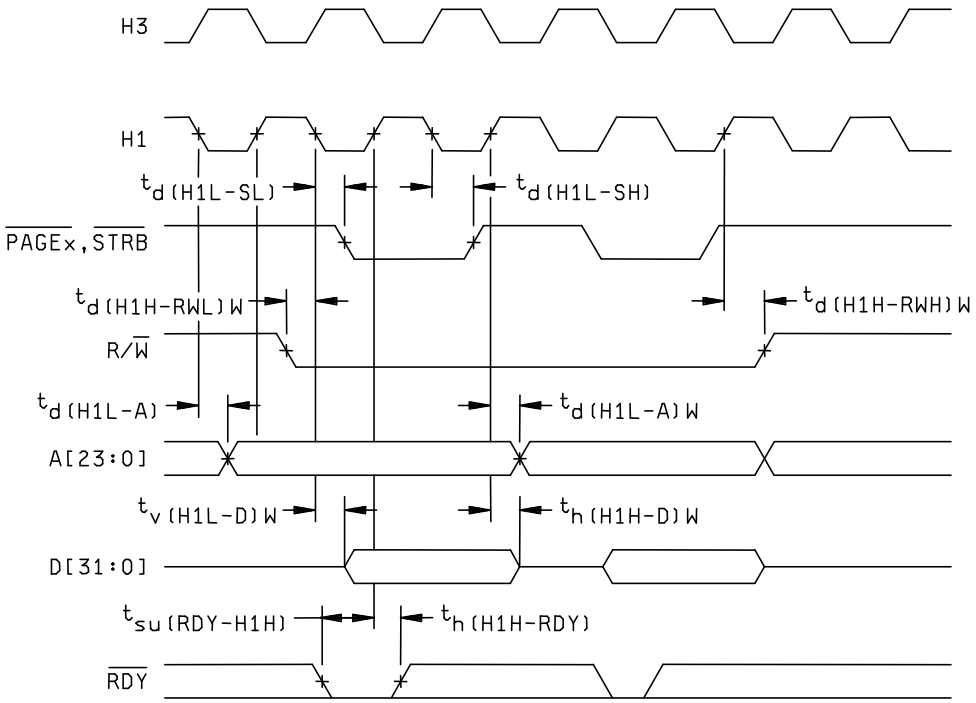
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR MEMORY ($\overline{STRB}$=0 AND $\overline{PAGEx}$=0) READ

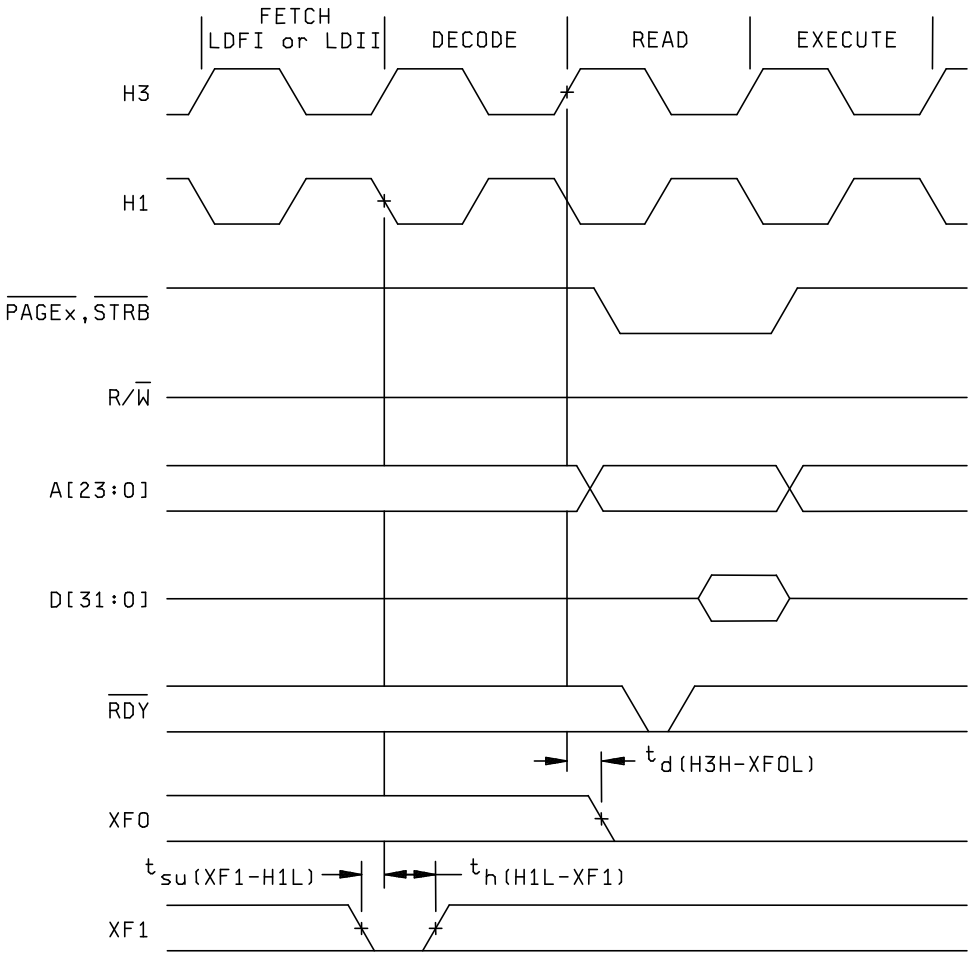
NOTE: $\overline{STRB}$ remains low during back-to-back read operation.

FIGURE 4. Test circuit and timing waveforms - Continued.



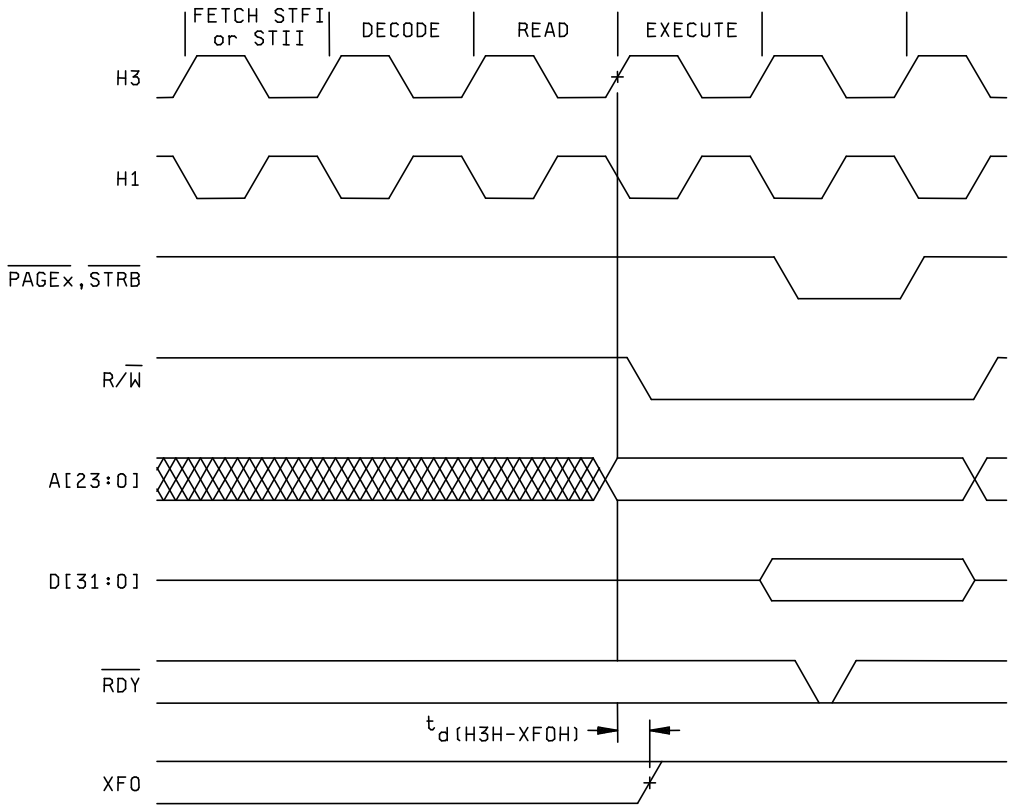
TIMING FOR MEMORY ($\overline{STRB}$=0 AND $\overline{PAGEx}$=0) WRITE

FIGURE 4. Test circuit and timing waveforms - Continued.



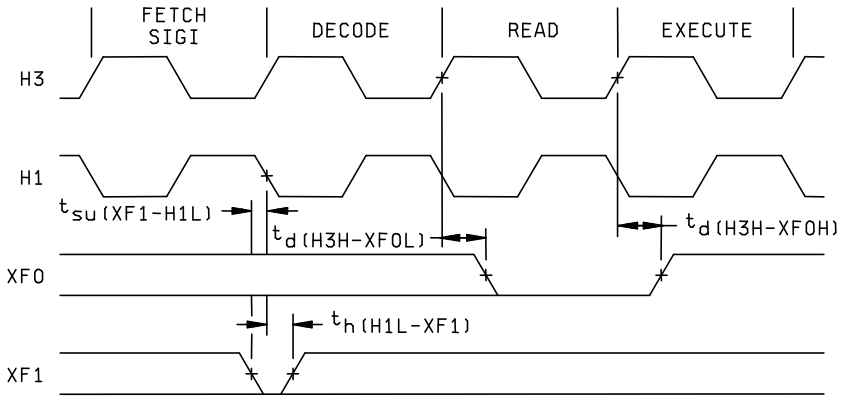
TIMING FOR XFO AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4. Test circuit and timing waveforms - Continued.

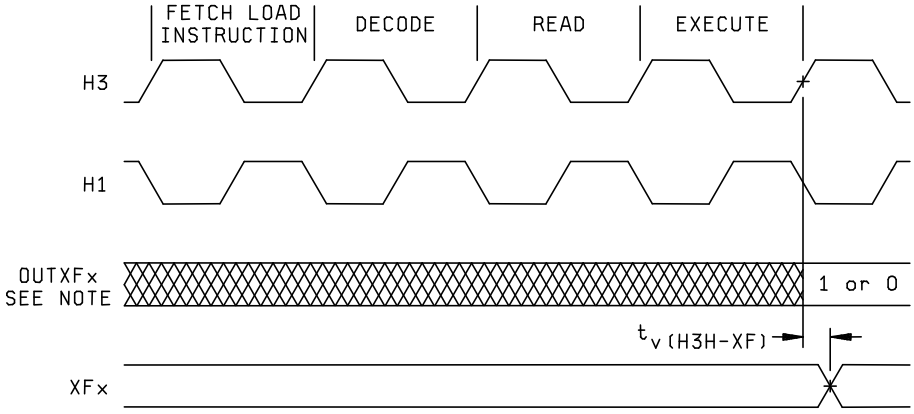


TIMING FOR XFO WHEN EXECUTING AN STFI OR STII

FIGURE 4. Test circuit and timing waveforms - Continued.



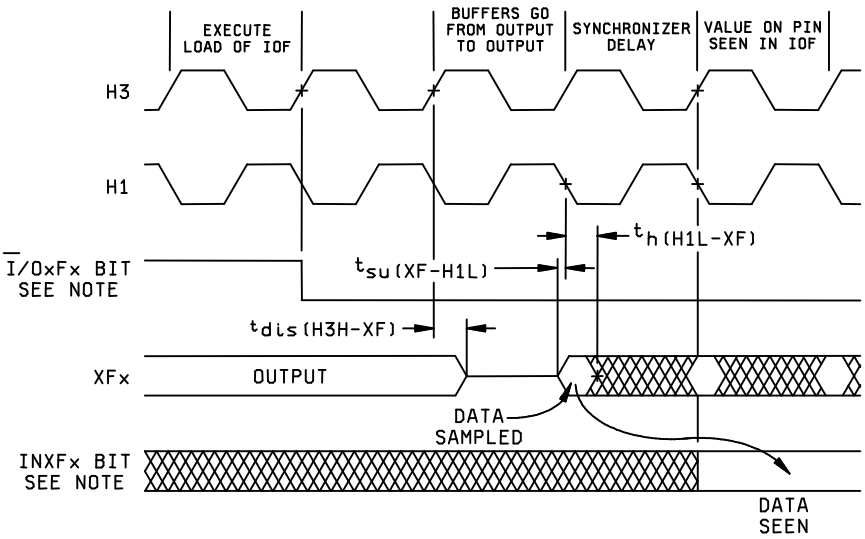
TIMING FOR XF0 AND XF1 WHEN EXECUTING SIGI



TIMING FOR LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

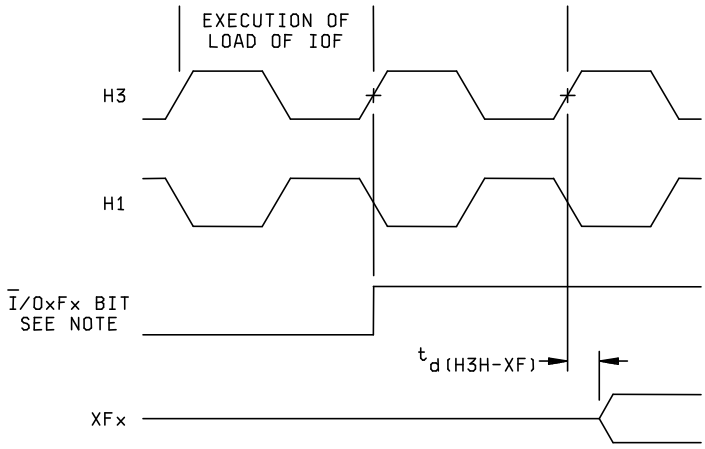
NOTE: OUTXFx represents either bit 2 or 6 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR CHANGING XFx FROM OUTPUT TO INPUT MODE

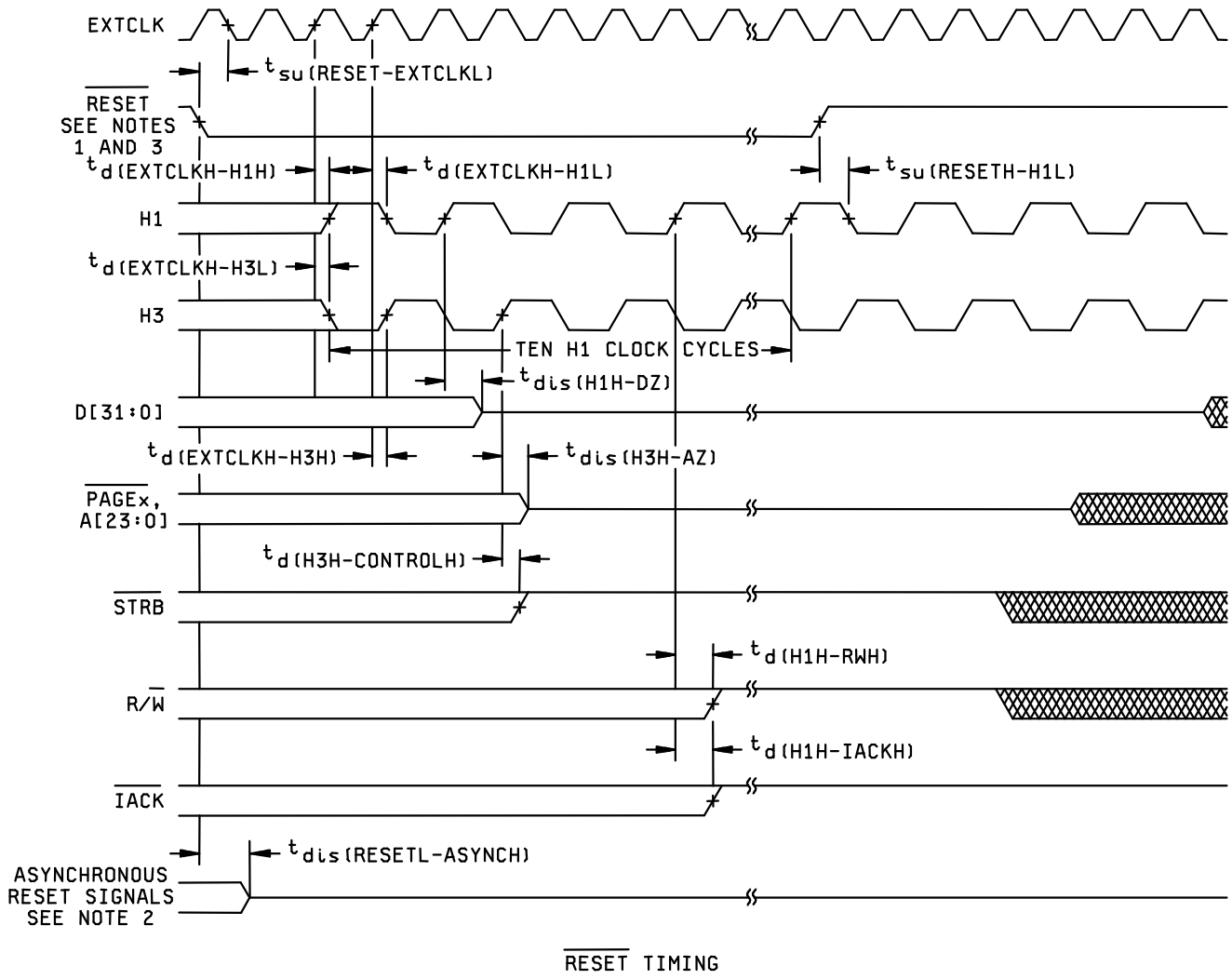
NOTE: $\overline{I}$/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of ther IOF register.



TIMING FOR CHANGING XFx FROM INPUT TO OUTPUT MODE

NOTE: $\overline{I}$/OxFx represents either bit 1 or bit 5 of the IOF register.

FIGURE 4. Test circuit and timing waveforms - Continued.

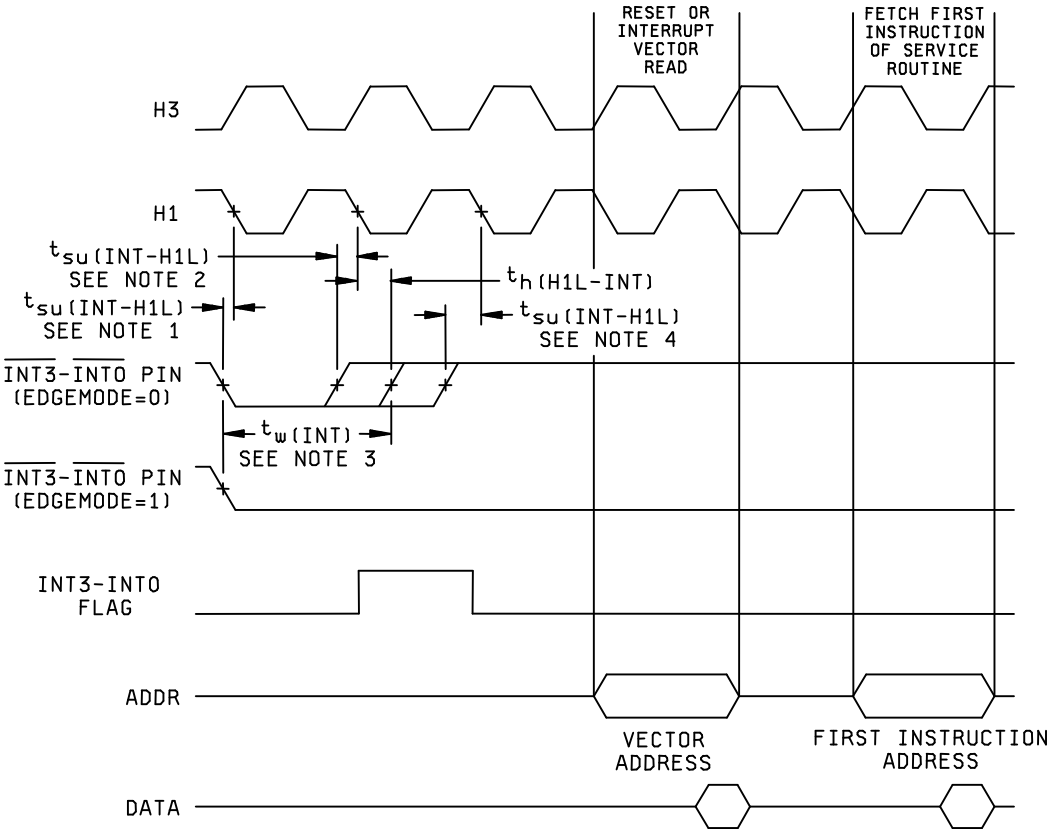


RESET TIMING

NOTES:

1. Clock circuit is configured in 'C31-compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H3.
2. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
3. $\overline{\text{RESET}}$ is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
4. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
5. The address and $\overline{\text{PAGE3}}$ - $\overline{\text{PAGE0}}$ outputs are placed in a high-impedance state during reset requiring a nominal 10-22 kΩ pullup. If not, undesirable spurious reads can occur when these outputs are not driven.

FIGURE 4. Test circuit and timing waveforms - Continued.



INT3-INT0 RESPONSE TIMING

NOTES:

1. Falling edge of H1 just detects $\overline{\text{INTx}}$ falling edge.
2. Falling edge of H1 detects second $\overline{\text{INTx}}$ low, however flag clear takes precedence.
3. Nominal width.
4. Falling edge of H1 misses previous $\overline{\text{INTx}}$ low as $\overline{\text{INTx}}$ rises.

FIGURE 4. Test circuit and timing waveforms - Continued.

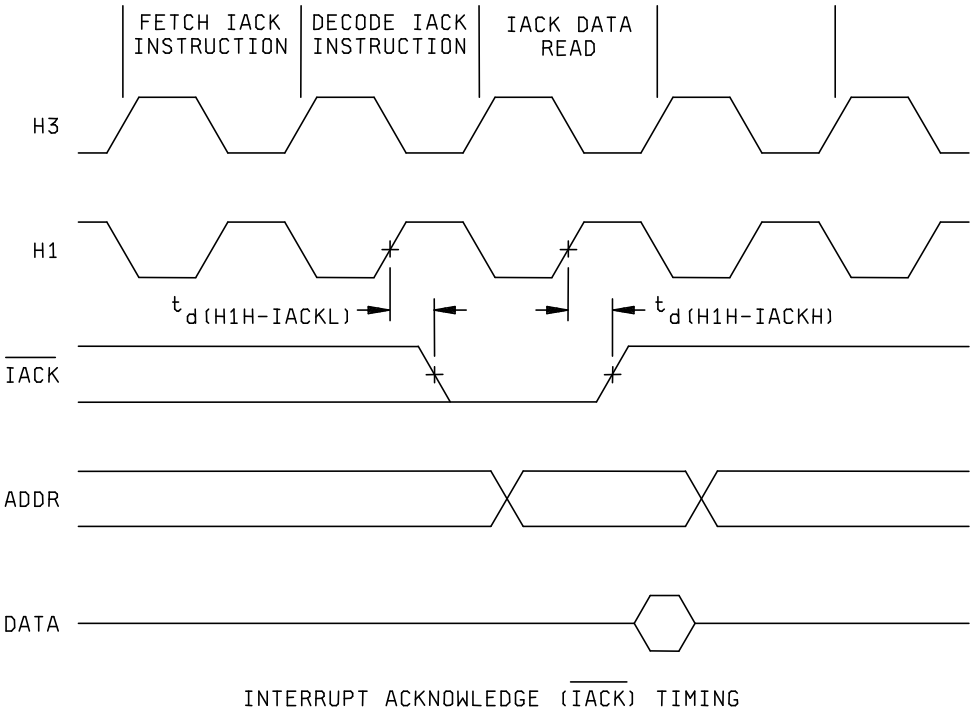
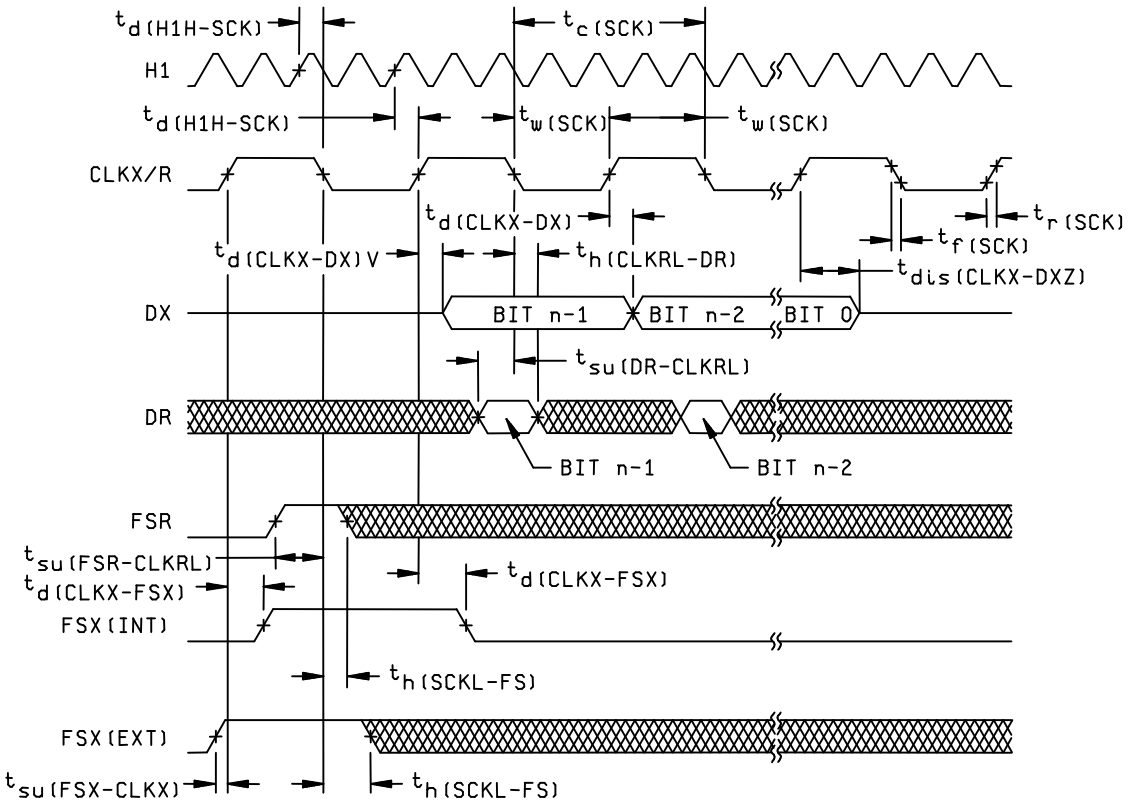


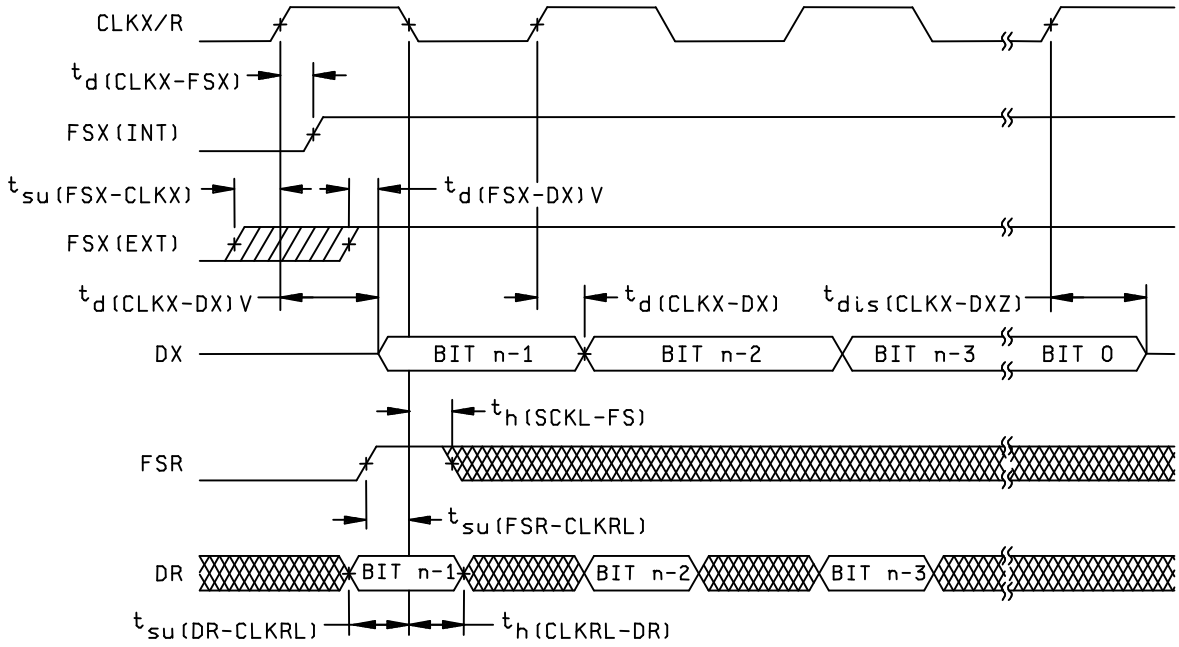
FIGURE 4. Test circuit and timing waveforms - Continued.



FIXED DATA-RATE MODE TIMING

NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

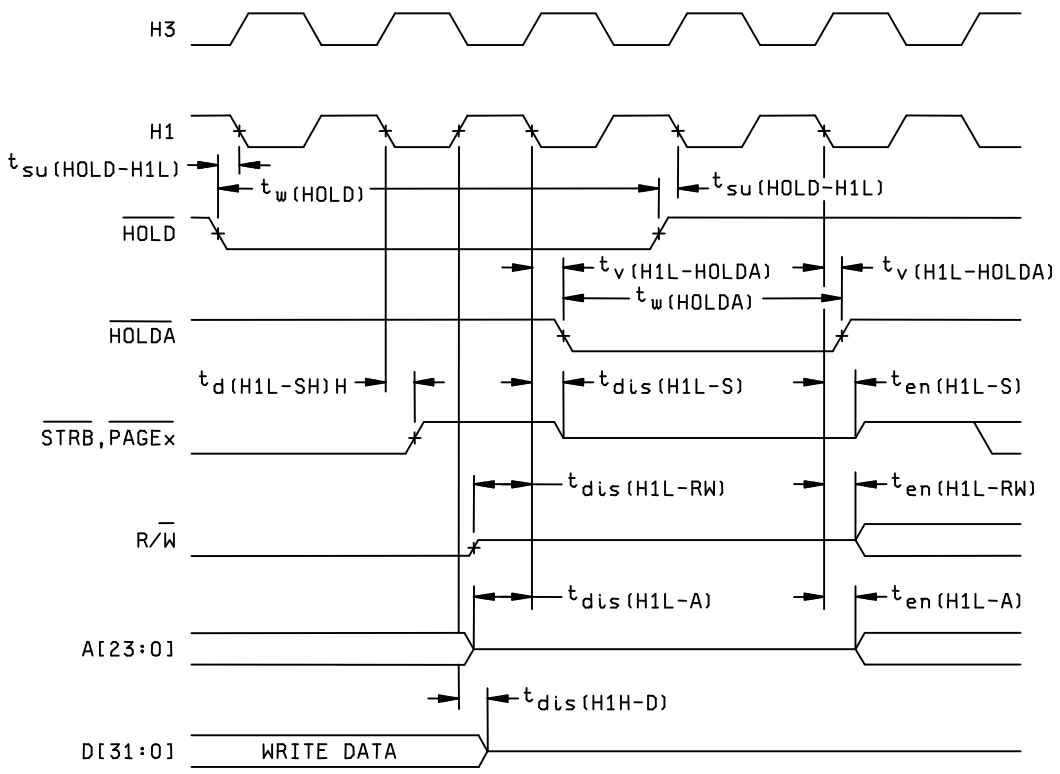
FIGURE 4. Test circuit and timing waveforms - Continued.



VARIABLE DATA-RATE MODE TIMING

NOTES:
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

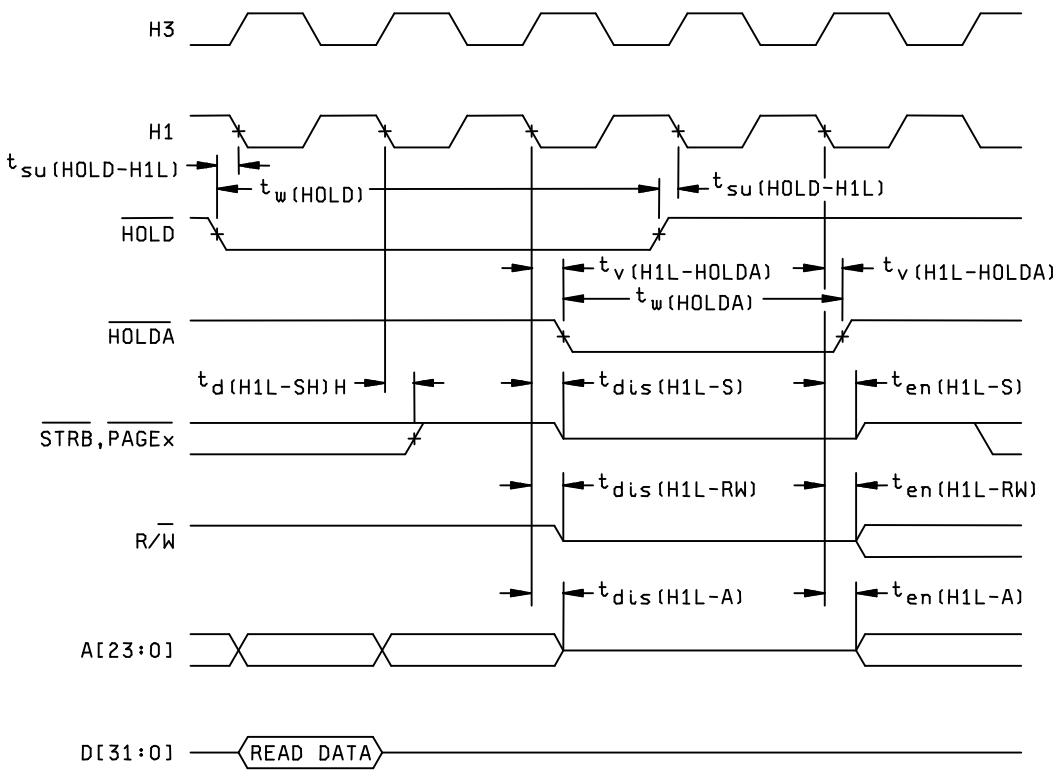
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (AFTER WRITE)

NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

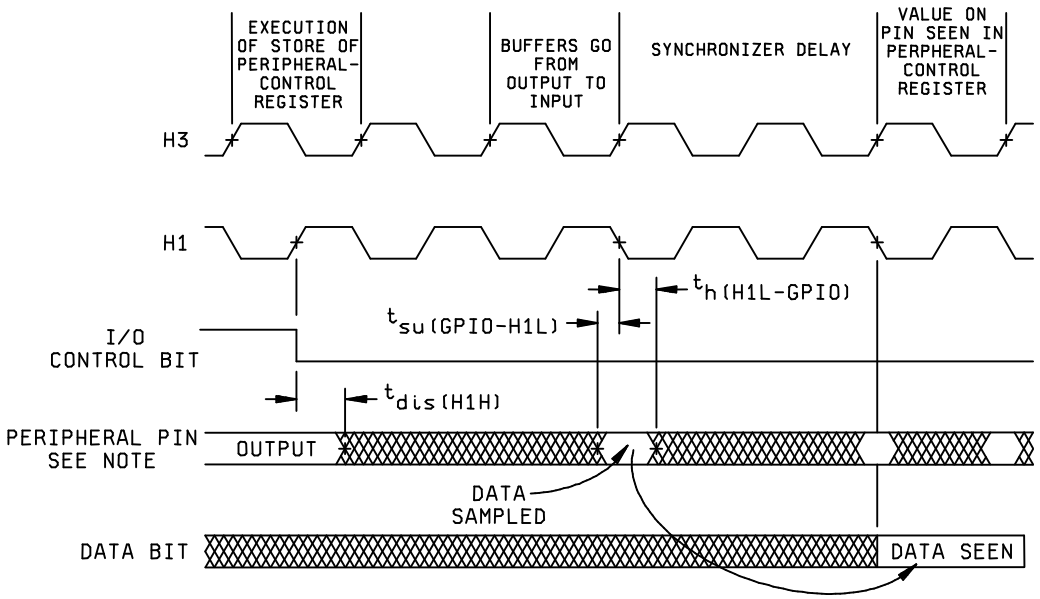
FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (AFTER READ)

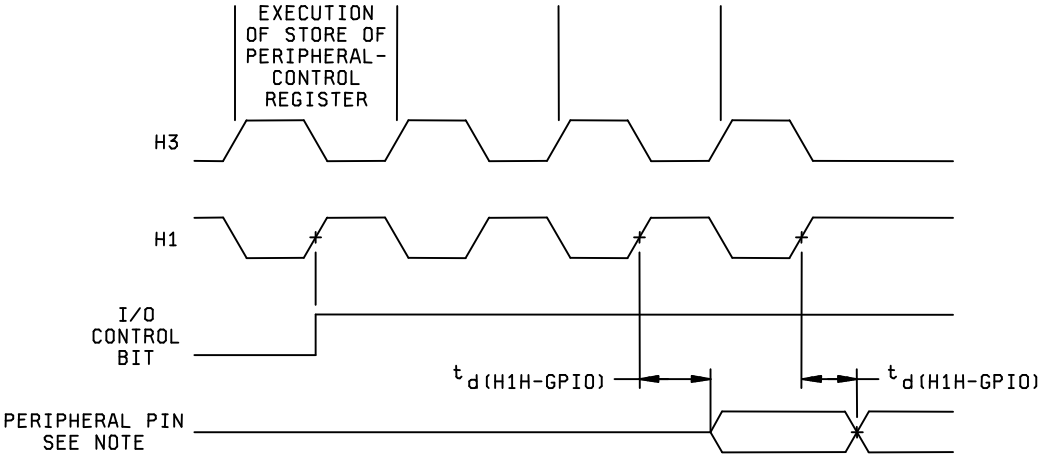
NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

FIGURE 4. Test circuit and timing waveforms - Continued.



CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE OUTPUT TO INPUT MODE TIMING

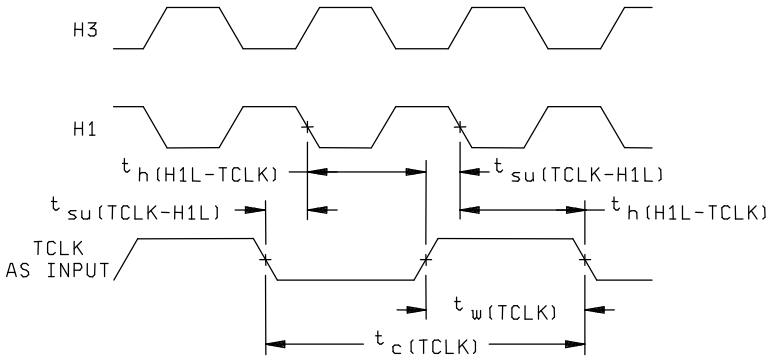
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.



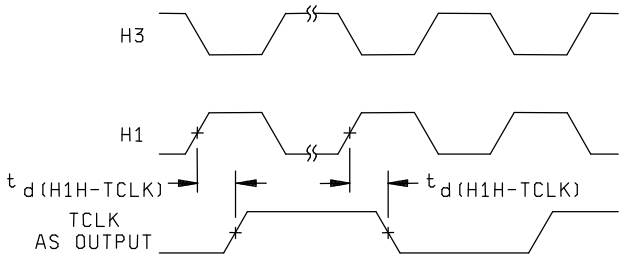
CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE INPUT TO OUTPUT MODE TIMING

NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

FIGURE 4. Test circuit and timing waveforms - Continued.

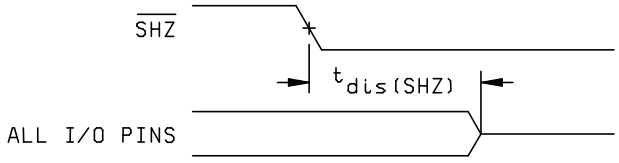


TIMER PIN TIMING,INPUT



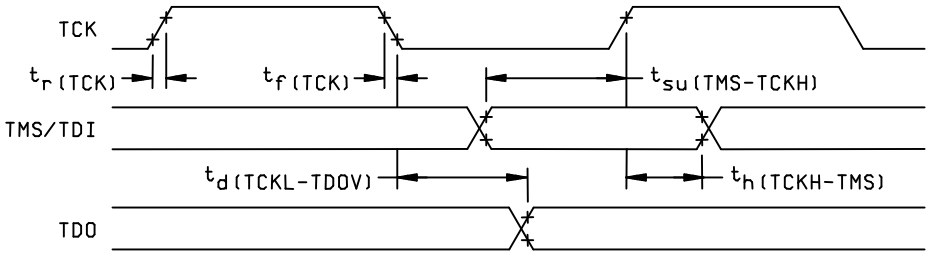
TIMER PIN TIMING,OUTPUT

FIGURE 4. Test circuit and timing waveforms - Continued.



TIMING FOR $\overline{SHZ}$

NOTE: Enabling $\overline{SHZ}$ destroys the device register and memory contents. Assert $\overline{SHZ}$ = 1 and reset the device to restore it to a known condition.



TEST ACCESS PORT TIMINGS

FIGURE 4. Test circuit and timing waveforms - Continued.

Instruction name	Instruction code	
EXTEST	00000000	
BYPASS	11111111	
SAMPLE	00000010	Boundary is only one dummy cell
HIGHZ	00000110	Boundary is only one dummy cell
PRIVATE1 1/	00000011	
PRIVATE2 1/	00100000	
PRIVATE3 1/	00100001	
PRIVATE4 1/	00100010	
PRIVATE5 1/	00100011	
PRIVATE6 1/	00100100	
PRIVATE7 1/	00100101	
PRIVATE8 1/	00100110	
PRIVATE9 1/	00100111	
PRIVATE10 1/	00101000	
PRIVATE11 1/	00101001	

1/ Use of private opcodes could cause the device to operate in an unexpected manner.

FIGURE 5. Boundary scan instruction code.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Terminal functions. The terminal functions used herein are defined in the following table II.

TABLE II. Terminal functions.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Primary-bus interface			
D31 – D0	I/O/Z	32-bit data port.	S H R
		Data port bus keepers.	S
A23 – A0	O/Z	24-bit address port.	S H R
R/$\overline{W}$	O/Z	Read/Write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over ther parallel interface.	S H R
$\overline{STRB}$	O/Z	Strobe. For all external-accesses.	S H
$\overline{PAGE0}$ - $\overline{PAGE3}$	O/Z	Page strobes. Four decoded page strobes for external access.	S H R
$\overline{RDY}$	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.	
$\overline{HOLD}$	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23 – A0, D31 – D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	

See footnotes at end table.

TABLE II. Terminal functions - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Primary-bus interface – Continued			
$\overline{\text{HOLDA}}$	O/Z	Hold acknowledge. $\overline{\text{HOLDA}}$ is generated in response to a logic-low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23 – A0, D31 – D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic-high of $\overline{\text{HOLD}}$ or the NOHOLD bit of the primary-bus-control register is set.	S
Control signals			
$\overline{\text{RESET}}$	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.	
EDGEMODE	I	Edge mode. Enables interrupt edge mode detection.	
$\overline{\text{INT3}}$ - $\overline{\text{INT0}}$	I	External interrupts.	
$\overline{\text{IACK}}$	O/Z	Internal acknowledge. $\overline{\text{IACK}}$ is generated by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate when a section of code is being executed.	S
MCBL/$\overline{\text{MP}}$	I	Microcomputer bootloader/microprocessor mode-select.	
$\overline{\text{SHZ}}$	I	Shutdown high impedance. When active, $\overline{\text{SHZ}}$ places all pins in the high-impedance state. $\overline{\text{SHZ}}$ can be used for board-level testing or to ensure that no dual-drive conditions occur. **Caution:** A low on $\overline{\text{SHZ}}$ corrupts the device memory and register contents. Reset the device with $\overline{\text{SHZ}}$ high to restore it to a known operating condition.	
XF1, XF0	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R
Serial port 0 signals			
CLKR0	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S R
CLKX0	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DR0	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S R
DX0	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSR0	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S R
FSX0	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S R

See footnotes at end table.

TABLE II. Terminal functions - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
Timer signals			
TCLK0	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S R
TCLK1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S R
Supply and oscillator signals			
H1	O/Z	External H1 clock.	S
H3	O/Z	External H3 clock.	S
CV_{DD}	I	$+V_{DD}$. Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane. 3/	
DV_{DD}	I	$+V_{DD}$. Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane. 3/	
V_{SS}	I	Ground. All grounds must be connected to a common ground plane.	
$PLLV_{DD}$	I	Internally isolated PLL supply. Connect to CV_{DD} (1.8 V).	
$PLLV_{SS}$	I	Internally isolated PLL ground. Connect to V_{SS}.	
EXTCLK	I	External clock. Logic level compatible clock input. If the XIN/XOUT oscillator is used, tie this pin to ground.	
XOUT	O	Clock out. Output from the internal-crystal oscillator. If a crystal is not used, XOUT should be left unconnected.	
XIN	I	Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground.	
CLKMD0, CLKMD1	I	Clock mode select pins.	
RSV0, RSV1	I	Reserved. Use individual pullups to DV_{DD}.	
JTAG emulation			
EMU1, EMU0	I/O	Emulation pins 0 and 1. Use individual pullups to DV_{DD}.	
TDI	I	Test data input.	
TDO	O	Test data output.	
TCK	I	Test clock.	
TMS	I	Test mode select.	
$\overline{TRST}$	I	Test reset.	

1/ I = input, O = output, Z = high-impedance state.

2/ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active.

3/ Recommended decoupling. Four 0.1 µF for CV_{DD} and eight 0.1 µF for DV_{DD}.

6.4 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03610-01XE	01295	SM320VC33PGEA120EP	SM320VC33PGEA120EP
V62/03610-02YE	01295	SM320VC33GNMM150EP	SM320VC33GNMM150EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493